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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,336	12/12/2003	Hea-Suk Jung	51876P428	3786

8791 7590 07/13/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN  
12400 WILSHIRE BOULEVARD  
SEVENTH FLOOR  
LOS ANGELES, CA 90025-1030

EXAMINER

WAMBACH, MARGARET R

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/735,336	JUNG, HEA-SUK	
	<b>Examiner</b>	<b>Art Unit</b>	
	Margaret R. Wambach	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 5/19/05
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☒ Claim(s) 2-8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>6/13/05</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Information Disclosure Statement*

It is noted that the reference cited on the 6/13/05 IDS included a translation of the abstract only. The examiner has ordered a translation of the entire document which was not yet available at the time that this office action was prepared. The claims will be reviewed in light of this document once it has been translated in its entirety.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnston et al hereafter "Johnston").

Referring to Figure 1 of Johnston, a clock divider is taught comprising a clock dividing means (102, 106, 108, 110, 112, 114, 120, 128 and 136) for receiving a source clock (REFERENCE CLOCK) to generate a plurality of divided clocks (from 120, 128, 136 and also 110, 112, 114 insofar as the signals input <sup>to</sup> the shift registers have been divided by 120 during previous iterations of the phase locked loop.)

With regard to the limitation that each divided clock has a different period, attention is directed to column 4 lines 50-67 of Johnston which specifically discloses an embodiment in which such would be the case. More particularly, Johnston discloses that the divided clock signals are intended for separate clock domains "where each

clock domain may differ from the operating frequencies of other clock domains within the integrated circuit.” Since period and frequency are inversely proportional, it follows that the period of each clock domain may differ from the operating period of other clock domains. Therefore, if the clock domains of the devices under test all required different periods, as suggested by Johnston, then the periods produced by the divided clocks would be different insofar as Johnston indicates that the dividers are designed to match the clock domains to which they supply clock signals.

Johnston also teaches test mode clock providing means (Multiplexers 130 and 138) for selectively outputting the plurality of the divided clocks in a test mode in response to a test mode signal (SCAN/TEST NORMAL);

and normal mode clock providing means for outputting selected one of the plurality of the divided clocks in a normal mode in response to the test mode signal (test and normal mode operation wherein the outputs are derived from shift registers 110, 112 and 114 is described in the last paragraph of column 6, for instance.)

What is not taught by Johnston is that the clock divider be “of a DLL” and that the source clock be “of the DLL”. In contrast, Johnston is incorporated into a phase lock loop (or PLL) and its clock dividing means receives the source clock of the PLL. To achieve the structure of claim 1, Johnston would have to be modified such that its clock dividing means, test mode clock providing means and normal mode clock providing means was incorporated into a DLL rather than a PLL. (Both PLL’s and DLL’s are used to suppress skew and jitter in clocks. The phase error of a PLL is accumulated while such is not the case for a DLL, resulting in lower jitter.) The primary elements of a phase

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lock loop are a VCO (voltage controlled oscillator) and a phase detector coupled in a feedback arrangement with the output coming from the VCO. A DLL typically has a VCDL (voltage controlled delay line) and phase detector also in a loop with the output coming from the VCDL. A substitution in the case of Johnston would be achieved by replacing VCO 108 by a VCDL. Motivation for such a substitution is provided by the fact that, as noted above, PLL's and DLL's are both typically used to produce clock signals but, as also noted above, DLL's are often preferable because the resulting clock signal is lower in jitter.

#### ***Allowable Subject Matter***

Claims 2-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Margaret R. Wambach whose telephone number is (571)272- 1756. The examiner can normally be reached on Monday, Tuesday, Thursday and Friday 6am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Margaret R Wambach  
Primary Examiner  
Art Unit 2816

mrw